Technical Annex No. 1

as of Dec 18, 2008 to the certification report
T-Systems-DSZ-CC-04164/04165-2008 as of July 11, 2008

ACOS EMV-A04V1 Configuration A and Configuration B

1 Scope of this annex

[1] This annex confirms the validity of the above mentioned certification report under the following circumstance:

- De-activation of the “"Inverse EEPROM Error Correction Attack Detection" (option in the order form of the underlying chip NXP SmartMX P5CC037V0A).

2 Justification

[2] The above change has been intensively investigated by the evaluators in additional tests.

[3] These tests have been documented by the evaluation facilty in an Observation Report, version 1.0 as of Dec 15, 2008.

3 Stipulations and Recommendations

[4] The stipulations for the *sponsor* as well as stipulations and recommendations *for the secure usage* of the TOE contained in the certification report T-Systems-DSZ-CC-04164/04165-2008 remain valid for the TOE with the change described in section 1.

4 Conclusion

[5] The certification of ACOS EMV-A04V1 Configuration A and Configuration B can be maintained under the change described in section 1.

End of Technical Annex No. 1 to T-Systems-DSZ-CC-04164/04165-2008.